

TECHNICAL NOTE

MEMORY MODULE SERIAL PRESENCE-DETECT

Introduction

Dynamic Random Access Memory (DRAM) technology at both the device and module level continues to grow in complexity. The presence-detect function for memory modules reflects this complexity.

When system power is applied, a computer's basic input/output system (BIOS) activates. The BIOS runs a command program that, among other things, detects the presence and function of subsystems that make up the computer. One of these subsystems is the computer's memory. Early memory modules relied on a parallel presence-detect function to communicate with a computer's BIOS. As module technology progressed, functional limits of parallel presence-detect led to the development of serial presence-detect (SPD).

Parallel Presence vs. Serial Presence-Detect Function

Parallel presence-detect utilized four to 10 module-edge connector pins to set a combination of high and low signals that defined unique module configurations, which was detected by the BIOS. The BIOS contained a memory truth table that translated these data bits into information on module density, speed, and other critical performance parameters. Micron used eight edge connector pins to create an eight-bit parallel presence-detect.

The main disadvantages of parallel presence-detect are:

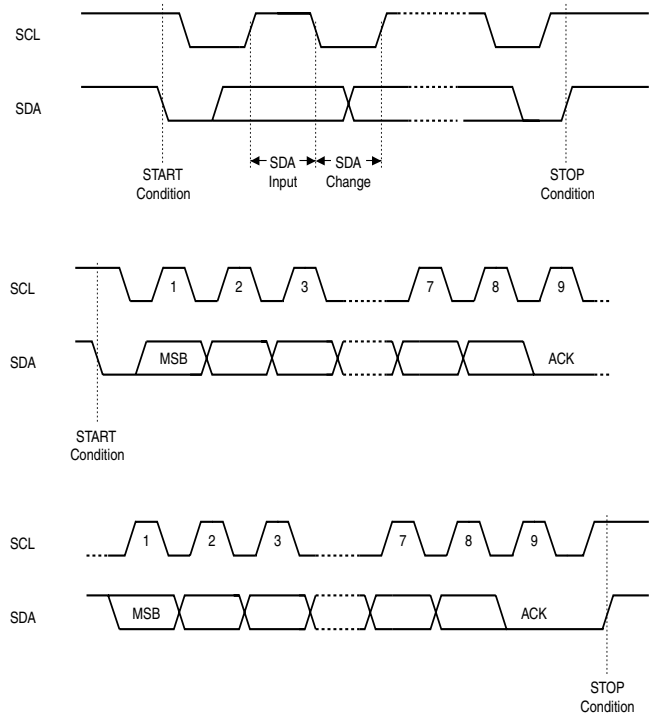
- addition of presence-detects bits requires additional edge connector pinouts;
- parallel presence-detect memory truth tables fixed the values of several presence-detect bits across a range of module types; this reduced the ability to identify specific module and device characteristics within the eight-bit limit.

SPD uses a separate, electronically erasable/programmable, read-only memory (EEPROM) device to hold module density, timing, and performance parameters.

Micron EEPROMs contain 256 bytes of programmable memory. Bytes 0 through 127 are programmed by Micron. Bytes 128 through 255 are reserved for module customers.

JEDEC has established I²C serial interface communication protocol to define SPD operations. This two-wire protocol is designed to minimize EEPROM pin count and simplify module printed circuit board (PCB) layout. Figure 1 summarizes I²C Bus Protocol. The primary advantage using SPD is with a fixed 8-pin footprint, the EEPROM contains a much larger (and more detailed) presence-detect data table.

Figure 1: I²C Bus Protocol



SPD Function

The module edge-connector pins used to operate the EEPROM consist of:

- serial clock (SCL)
- serial data (SDA)
- write protect (WP)
- three address inputs (SA0–SA2)

The SCL input is used to clock all data into and out of the device. SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wired as logic "OR" with any number of other SDA

Table 1: Device Select Code

The most significant bit (b7) is sent first

					CHIP ENABLE			R \bar{W}
	b7	b6	b5	b4	b3	b2	b1	b0
Memory Area Select Code (two arrays)	1	0	1	0	SA2	SA1	SA0	R \bar{W}
Protected Register Select Code	0	1	1	0	SA2	SA1	SA0	R \bar{W}

pins. The WP pin is the hardware write protect pin. The SA0, SA1 and SA2 address pins are connected to VDD or VSS to configure the EEPROM address.

As specified by the I²C memory standard, each EEPROM contains a built-in 4-bit Device Type Identifier code (1010), and a second Device Type Identifier Code (0110) to access the Protection Register. These codes are used together with one of three alternative addressing methods to select memory modules attached to the I²C bus, as shown in Table 1, Device Select Code. Each module's EEPROM behaves as a slave device in the I²C protocol, with all EEPROM memory operations synchronized by the serial clock.

Clock and Data Conventions

Data states on the SDA line can only change during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating stop and start conditions.

Start/Stop Conditions

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The SPD continuously monitors the SDA and SCL lines for start conditions and will not respond to any command until this condition is met.

All communications are terminated by a stop condition, which a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the SPD to place the device in standby power down mode.

Acknowledge

Acknowledge (Ack) is a software convention used to indicate successful data transfers. The transmitting device, either master or slave will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line low to acknowledge that it received the eight bits of data.

The SPD will always respond with an Ack after recognition of a start condition and its slave address. If both the device and write operation are selected, the SPD will respond with an Ack after the receipt of each subsequent eight-bit word.

In the read mode, the SPD slave will transmit eight bits of data, release the SDA line and monitor the line for an Ack. If an Ack is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an Ack is not detected, the slave will terminate further data transmissions and wait for a stop condition to return to standby power mode.

The serial EEPROM has a software write protect feature that allows the lower half of the array (bytes 0-128) to be permanently write protected. This feature is invoked by writing to the write protect register. Once the software write protect register has been written, the write protection is enabled and cannot be reversed, even if the device is powered down. For hardware write protection the WP pin can be tied to VDD and the entire array will be write protected, regardless of whether the software write protect register has been written or not. If the WP pin is set to VDD, it will prevent the software write protect register from being written.

To facilitate production flexibility ease of module rework, Micron does not write protect the lower half of the SPD, unless specifically requested by a customer. In addition, for all Micron memory modules, the EEPROMs WP pin is tied to VSS, disabling the hardware write protect for the entire SPD.

SPD Addressing and System Design

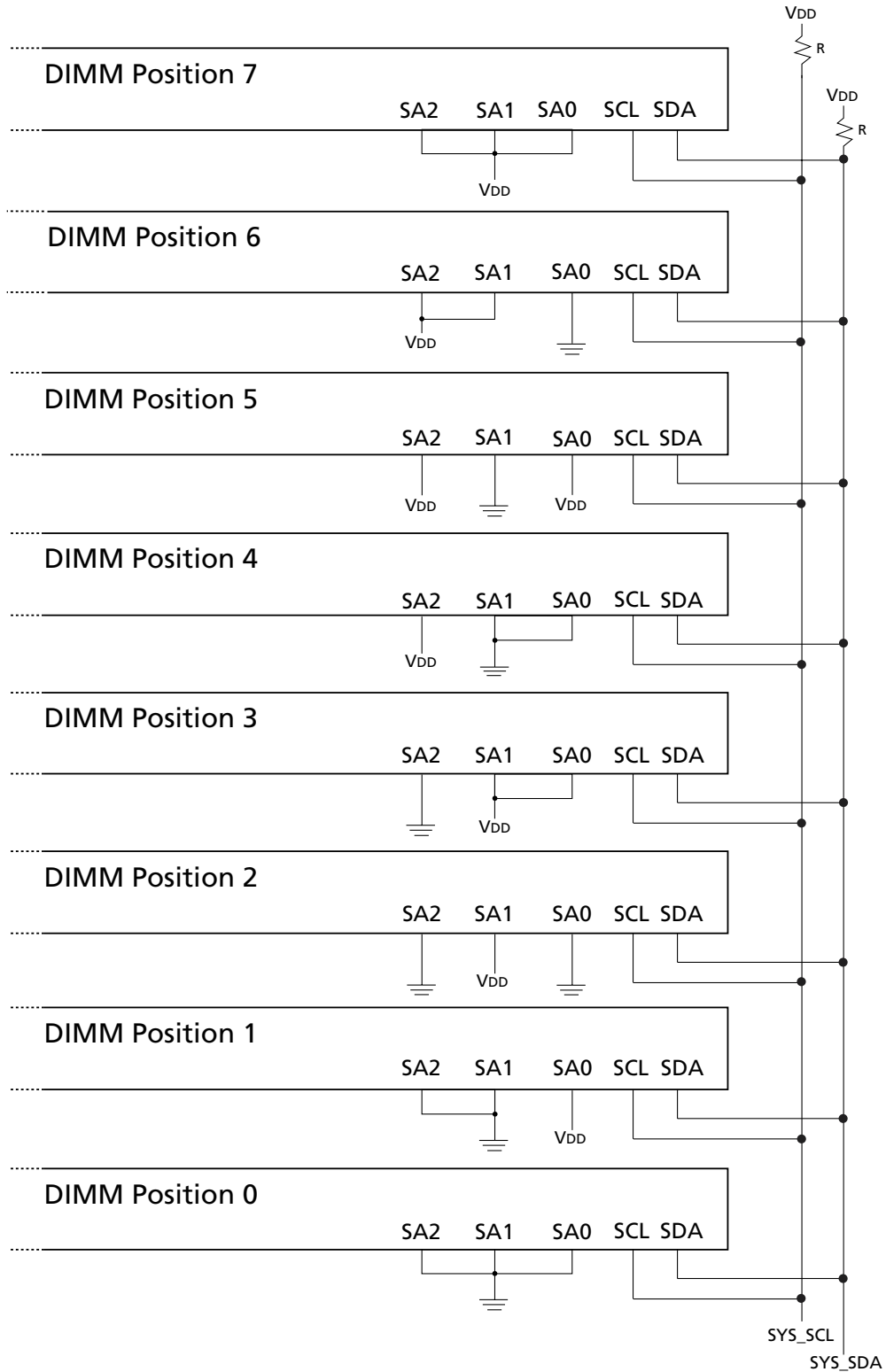
The SPD addressing can be incorporated into a system design in three ways:

- Common Clock/Common Data
- Common Clock/Separate Data
- Common Data/Separate Clock

Common Clock/Common Data

In this configuration, SA0–SA2 are wired in a binary sequence at each DIMM socket for a maximum of eight modules, as shown in Figure 2, SPD Block Diagram (Common Clock/Common Data), on page 3. All eight modules share a common clock and common data line. Pull-up resistors (4.7K typical) are required on all SCL and SDA signals due to their open drain interface.

Figure 2: SPD Block Diagram (Common Clock/Common Data)

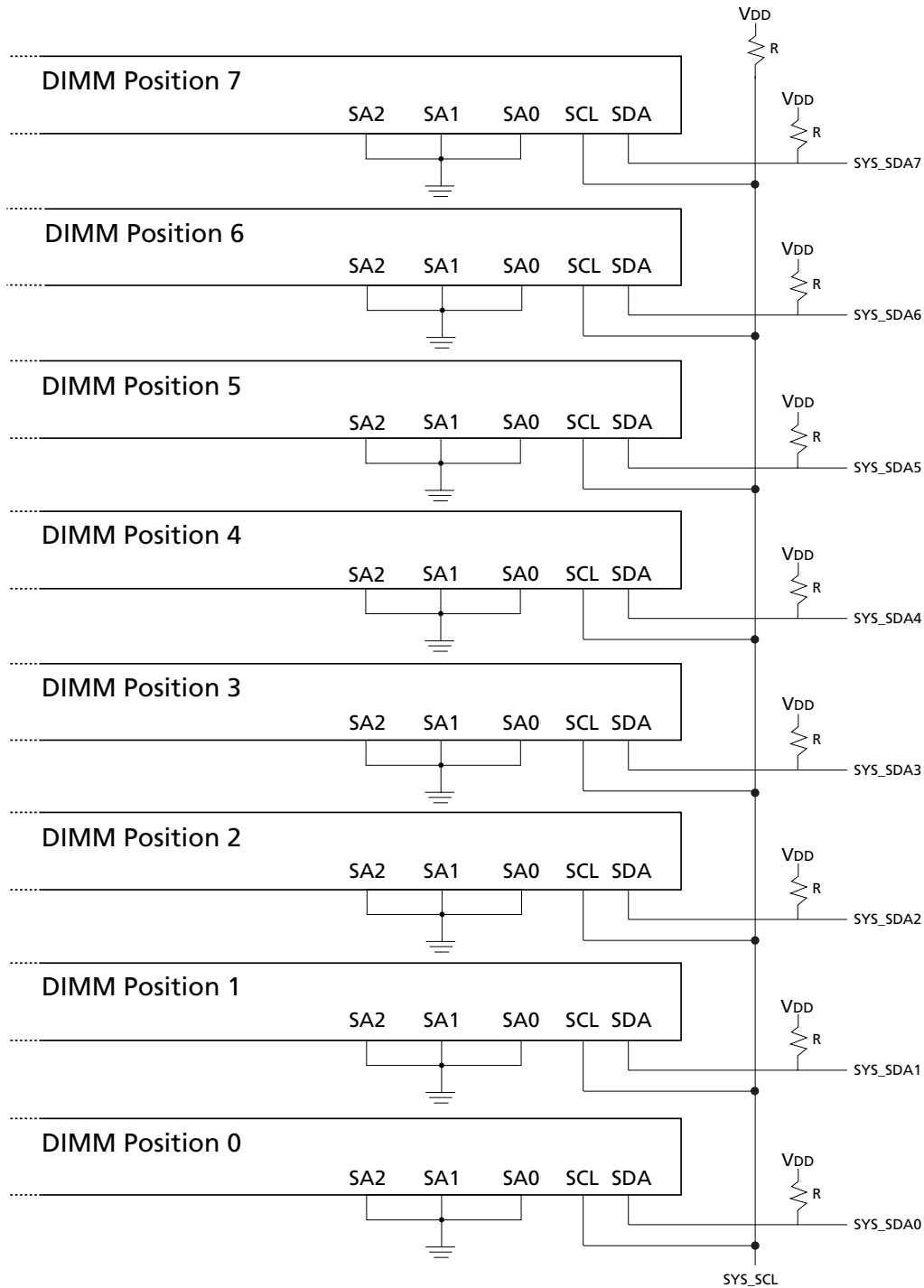


Common Clock/Separate Data

In this configuration, SA0–SA2 are wired to the same address at each DIMM socket (typically all to Vss), as shown in Figure 3, SPD Block Diagram (Common Clock/Separate Data). The SCL is wired to all positions.

The SDA is unique for each position, allowing for greater than eight positions, but not permitting C_{MAX} to exceed 400pf. Since the data pins are separate, eight positions could provide parallel data paths of one byte (8x speed improvement).

Figure 3: SPD Block Diagram (Common Clock/Separate Data)

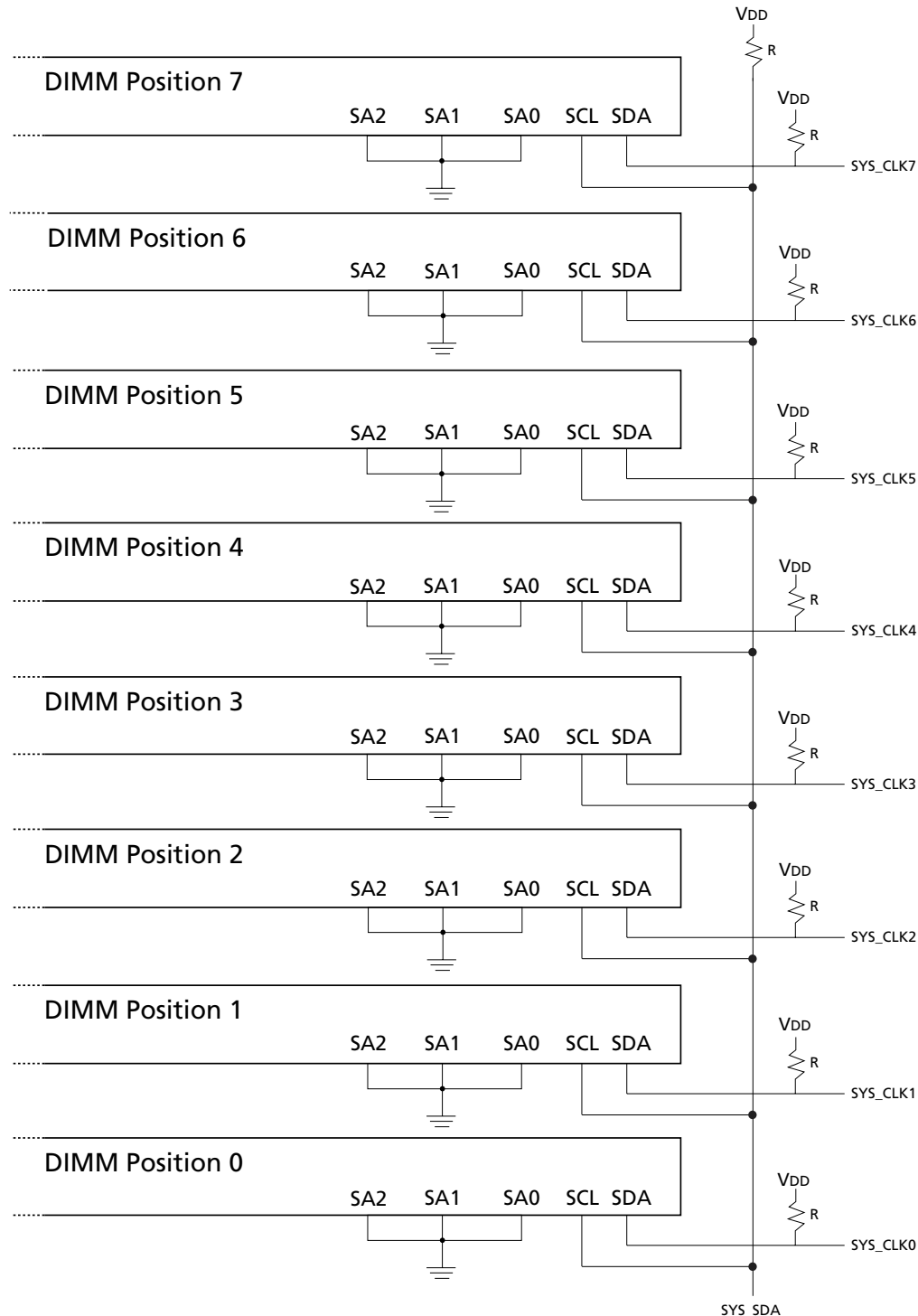


Common Data/Separate Clock

SA0-SA2 are wired at each DIMM to the same address, as shown in Figure 4, SPD Block Diagram (Common Data/Separate Clock). The SDA is wired to

all positions. The SCL is unique for each position, allowing for greater than eight positions, but not permitting CMAX to exceed 400pF.

Figure 4: SPD Block Diagram (Common Data/Separate Clock)



Decimal to Binary to Hex conversions

Table 2, Decimal to Binary to Hex conversion, shows how to place a decimal value in a binary (0/1) format, and then create a hex value from binary.

In the Hexadecimal system, the eight bits of each byte are split into two sets of four nibbles each. The value generated from the bits in the upper nibble create the first hex character, while the bit values in the lower nibble generate the second hex character. Each nibble can have a maximum decimal value of 15. Hex values are: 00 through 09, 10 = 0A, 11 = 0B, 12 = 0C, 13 = 0D, 14 = 0E, and 15 = 0F. Following this sequence, adding one to 0x0F, results in 0x10 or 16 in decimal.

As shown below, the binary value of 45 results in a '2' in the upper hex nibble and '13' (or D) in the lower hex nibble. Thus, the hex value for 45 is 2D, usually displayed as 0x2D. If this looks familiar, it may be because ASCII is based in the hexadecimal numbering system.

Serial Presence-Detect Tables

All serial presence-detect tables have the same basic format. Bytes are numbered sequentially from 0 to 255, and each byte consists of eight data bits. These eight bits with either '0' or 1 values generate a byte's hex value. Each SPD byte has an associated data or look up table, showing which module parameter is represented. In some instances, the hex value directly represents a parameter. For example, SPD byte 0 has a hex value of 0x80, or decimal 128. Byte 0 represents the number of SPD bytes utilized by the module manufacturer. Micron utilizes the first 128 SPD bytes.

The majority of SPD bytes are associated with parameter look up tables. A byte's hex number will represent the parameters listed in the table, not just the numeric hex value.

SPD Data Tables

Following are examples of SPD data tables for each DRAM technology.

Table 2: Decimal to Binary to Hex conversion

		BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	OUTPUT
Binary Values	128	64	32	16	8	4	2	1	
	0	0	1	0	1	1	0	1	45
Hex Values	8	4	2	1	8	4	2	1	
	0	0	1	0	1	1	0	1	
	2				D				45

DRAM Serial presence-detect (EDO or Fast Page)

Table 3 is an example of a presence-detect table for EDO/Fast Page modules.

Table 3: EDO/FP DRAM Serial Presence-Detect Table

Hex values shown are representative

BYTE NUMBER	FUNCTION DESCRIBED	SPD HEX VALUE
0	Defines number of bytes written into serial memory at module mfg	80
1	Total number of SPD memory bytes	08
2	Fundamental memory type (FPM or EDO)	01 or 02
3	Number of row addresses on the memory device	0C
4	Number of column addresses on memory device	0A
5	Number of physical banks on this memory module	01
6	Data Width of this module	40
7	Data Width (continued)	00
8	Module voltage interface levels	01
9	RAS# access time of this assembly	3C
10	CAS# access time of this assembly	0F
11	Module error correction configuration type (Non-parity, Parity, ECC)	00 or 01 or 02
12	Refresh Rate/Type	00 or 83
13	Primary DRAM width	10
14	Error Checking DRAM data width	00
15–61	Reserved	00
62	SPD revision	00
63	Checksum for bytes 0–62	Calculated
64	Manufacturers JEDEC ID code	2C
65-71	Manufacturers JEDEC ID code (Continued)	FF
72	Manufacturing location	01 - 0C
73–90	Manufacturer's Part Number	Variable
91	PCB identification code	01 - 09
92	PCB identification code (continued)	00
93	Year of manufacture	Variable
94	Week of manufacture	Variable
95–98	Module Serial Number	Variable
99–125	Manufacturer Specific Data	Variable
126–127	Reserved	00
128–255	Open User Free-Form area not defined	FF

SDRAM Serial presence-detect

Table 4 is an example of a SDRAM module serial presence-detect table. SDRAM SPD tables are similar

to DRAM tables, but with additional byte locations that provide SDRAM device timing parameters and more module functional data.

Table 4: SDRAM Serial Presence-Detect Table

Hex values shown are representative.

BYTE NUMBER	FUNCTION DESCRIBED	SPD HEX VALUES
0	Number of bytes used by module manufacturer	80
1	Total number of SPD memory bytes	08
2	Fundamental memory type (SDRAM)	04
3	Number of SDRAM device row addresses	0C
4	Number of SDRAM device column addresses	0B
5	Number of physical banks on this SDRAM module	01
6	Module Data Width	40
7	Module Data Width (continued)	00
8	Voltage interface standard of this assembly	01
9	SDRAM Device Cycle Time t_{CK} (highest CAS latency CL=3)	75
10	SDRAM Device Access from Clock t_{AC} (highest CAS latency CL=3)	54
11	DIMM Configuration type (non-parity, ECC)	00 or 02
12	Refresh Rate/Type	80 or 82
13	Primary SDRAM Width	08
14	Error Checking SDRAM width	00
15	Minimum Clock Delay Back to Back Random Column Address t_{CCD}	01
16	Burst Lengths Supported (1, 2, 8, full page)	8F
17	Number of Banks in Each SDRAM Device	04
18	CAS# Latencies Supported (CL = 2 and 3)	06
19	CS# Latency (CS# latency = 0)	01
20	WE# Latency (WE# latency = 0)	01
21	SDRAM Module Attributes (see SDRAM SPD standard for value definitions)	00
22	SDRAM Device Attributes: General (see SDRAM SPD standard for value definitions)	0E
23	SDRAM Device Cycle Time t_{CK} at 2nd highest CAS latency (CL=2)	A0
24	SDRAM Device Access from Clock t_{AC} at 2nd highest CAS latency (CL=2)	60
25	SDRAM Device Cycle Time t_{CK} at 3rd highest CAS latency (not supported, see byte 18)	00
26	SDRAM Device Access from Clock t_{AC} at 3rd highest CAS latency (not supported, see byte 18)	00
27	SDRAM Device Minimum Row Precharge Time t_{RP}	14
28	SDRAM Device Minimum Row Active to Row Active t_{RRD}	0F
29	SDRAM Device Minimum RAS# to CAS# Delay t_{RCD}	14
30	SDRAM Device Minimum RAS# Pulse Width t_{RAS}	2C
31	Module Bank Density (see SDRAM SPD standard for value definitions)	20
32	SDRAM Device Command and Address signal input setup time t_{AS}	15
33	SDRAM Device Command and Address signal input hold time t_{AH}	08
34	SDRAM Device Data signal input setup time t_{DS}	15
35	SDRAM Device Data signal input hold time t_{DH}	08
36-61	Reserved	00
62	SPD Data Revision Code (current rev, 1.2b)	12
63	Checksum for bytes 0-62	Calculated
64	Manufacturer's JEDEC ID Code (Micron's is 44)	2C

Table 4: SDRAM Serial Presence-Detect Table (Continued)

Hex values shown are representative.

BYTE NUMBER	FUNCTION DESCRIBED	SPD HEX VALUES
65-71	Manufacturer's JEDEC ID Code (continued)	FF
72	Manufacturing Location	01-0C
73-90	Manufacturer's Part Number	Variable
91	PCB Identification Code	01-09
92	PCB Identification Code (continued)	00
93	Year of Manufacture	Variable
94	Week of Manufacture	Variable
95-98	Module Serial Number	Variable
99-125	Manufacturer Specific Data	Variable
126	Intel Specification for frequency (100 MHz)	64
127	Intel Specification Clock Lines, Junction Temp and CAS# Latency support	AF
128-255	Open User Free-Form area not defined	FF

DDR SDRAM Serial presence-detect

Table 5 is an example of a DDR SDRAM module serial presence-detect table. The DDR SDRAM SPD table has many of the same byte values seen in the SDRAM table, but with additional byte locations that

provide specific DDR device timing parameters. DDR SDRAM SPD specification is now at rev 1.0. As of July 31, 2003, all Micron DDR 400 modules conform to Intel specification rev. 1.1.

Table 5: DDR SDRAM Serial Presence-Detect Table

Hex values shown are representative

BYTE NUMBER	FUNCTION DESCRIBED	SPD HEX VALUE
0	Number of bytes used by module manufacturer	80
1	Total number of SPD memory bytes	08
2	Fundamental Memory Type (DDR SDRAM)	07
3	Number of DDR SDRAM device row addresses	0D
4	Number of DDR SDRAM device column addresses	0A
5	Number of physical ranks on this DDR SDRAM module	01
6	Module Data Width	40
7	Module Data Width (Continued)	00
8	Module Voltage Interface Level	04
9	DDR SDRAM Device Cycle Time t_{CK} (highest CAS latency CL = 2.5)	75
10	DDR SDRAM Device Access from Clock t_{AC} (highest CAS latency CL = 2.5)	75
11	DIMM Configuration type (non-parity, ECC)	00 or 02
12	Refresh Rate/Type	80 or 82
13	Primary DDR SDRAM Width	08
14	Error Checking DDR SDRAM Width	00
15	Minimum Clock Delay Back to Back Random Column Address t_{CCD}	01
16	Burst Lengths Supported (1, 2, and 8)	0E
17	Number of Banks in Each DDR SDRAM Device	04
18	CAS# Latencies Supported (CL = 2.5 and 3)	0C
19	\overline{CS} Latency (\overline{CS} latency = 0)	01
20	WE# Latency (WE# latency = 1)	02
21	DDR SDRAM Module Attributes (see DDR SPD standard for value definitions)	20
22	DDR SDRAM Device Attributes: General (see DDR SPD standard for value definitions)	C0
23	DDR SDRAM Device Cycle Time t_{CK} at 2nd highest CAS latency (CL = 2)	A0
24	DDR SDRAM Device Access from Clock t_{AC} at 2nd highest CAS latency (CL = 2)	75
25	DDR SDRAM Device Cycle Time t_{CK} at 3rd highest CAS latency (not supported, see byte 18)	00
26	DDR SDRAM Device Access from Clock t_{AC} at 3rd highest CAS latency (not supported, see byte 18)	00
27	DDR SDRAM Device Minimum Row Precharge Time t_{RP}	50
28	DDR SDRAM Device Minimum Row Active to Row Active t_{RRD}	3C
29	DDR SDRAM Device Minimum RAS# to CAS# Delay t_{RCD}	50
30	DDR SDRAM Device Minimum RAS# Pulse Width t_{RAS}	2D
31	Module Rank Density (see DDR SPD standard for value definitions)	40
32	DDR SDRAM Device Command and Address signal input setup time (Slow Slew Rate) t_{IS_s}	A0

Table 5: DDR SDRAM Serial Presence-Detect Table

Hex values shown are representative

BYTE NUMBER	FUNCTION DESCRIBED	SPD HEX VALUE
33	DDR SDRAM Device Command and Address signal input hold time (Slow Slew Rate) t_{IH_s}	A0
34	DDR SDRAM Device Data signal input setup time t_{DS}	50
35	DDR SDRAM Device Data signal input hold time t_{DH}	50
36-40	RESERVED	00
41	DDR SDRAM Device Minimum Active to Active/Auto Refresh Time t_{RC}	41
42	DDR SDRAM Device Minimum Auto-Refresh to Active/Auto-Refresh t_{RFC}	4B
43	DDR SDRAM Device Maximum device cycle time t_{CKMAX}	34
44	DDR SDRAM Device Maximum skew between DQS and DQ signals t_{DQSQ}	32
45	DDR SDRAM Device Maximum Read DataHold Skew Factor t_{QHS}	75
46	RESERVED	00
47	DDR SDRAM DIMM Height (see DDR SPD standard for value definitions)	01
48-61	RESERVED	00
62	SPD Revision (current rev, 1.0. For DDR 400, rev 1.1. shown as 0x11 per Intel spec.)	10 or 11
63	Checksum for Bytes 0-62	Calculated
64	Manufacturer's JEDEC ID Code (Micron's is 44)	2C
65-71	Manufacturer's JEDEC ID Code (Continued)	FF
72	Module Manufacturing Location	01-0C
73-90	Module Part Number	Variable
91	PCB Identification Code	01-09
92	PCB Identification Code (Continued)	00
93	Year of Manufacture	Variable
94	Week of Manufacture	Variable
95-98	Module Serial Number	Variable
99-127	Manufacturer's Specific Data	Variable
128-255	Open for customer use	FF

DDR2 SDRAM Serial Presence Detect

Table 6 is an example a DDR2 serial presence detect table. DDR2 is the latest development in DRAM Technology. The speed and complexity of DDR2 operation compared to DDR is reflected in the addition of several

device timing parameters to the SPD table. For detailed information on DDR2 device operating characteristics, see Micron's 256Mb or 512Mb DDR2 SDRAM data sheet. JEDEC has started DDR2 SPD standard at rev. 1.0.

Table 6: DDR2 SDRAM Serial Presence Detect Table

Hex values shown are representative

BYTE NUMBER	FUNCTION DESCRIBED	SPD HEX VALUE
0	Number of bytes used by module manufacturer	80
1	Total number of SPD memory bytes	08
2	Fundamental Memory Type (DDR2 SDRAM)	08
3	Number of DDR2 SDRAM device row addresses	0D
4	Number of DDR2 SDRAM device column addresses	0A
5	DIMM Height and Number of physical ranks (see DDR2 SPD standard for value definitions)	60
6	Module Data Width	40
7	RESERVED	00
8	Module Voltage Interface Level	05
9	DDR2 SDRAM Device Cycle Time t_{CK} (highest CAS latency CL= 4)	50
10	DDR2 SDRAM Device Access from Clock t_{AC} (highest CAS latency CL= 4)	60
11	DIMM Configuration type (non-parity, ECC)	00 or 02
12	Refresh Rate/Type	80 or 82
13	Primary DDR2 SDRAM Width	08
14	Error Checking DDR2 SDRAM Width	00
15	RESERVED	00
16	Burst Lengths Supported (4 and 8)	0C
17	Number of Banks in Each DDR2 SDRAM Device	04
18	CAS Latencies Supported (CL = 4 and 3)	18
19	RESERVED	00
20	DIMM Type Information (see DDR2 SPD standard for value definitions)	02
21	DDR2 SDRAM Module Attributes (see DDR2 SPD standard for value definitions)	00
22	DDR2 SDRAM Device Attributes: General (see DDR2 SPD standard for value definitions)	01
23	DDR2 SDRAM Device Cycle Time t_{CK} at 2nd highest CAS latency (CL = 3)	50
24	DDR2 SDRAM Device Access from Clock t_{AC} at 2nd highest CAS latency (CL = 3)	60
25	DDR2 SDRAM Device Cycle Time t_{CK} at 3rd highest CAS latency (not supported, see byte 18)	00
26	DDR2 SDRAM Device Access from Clock t_{AC} at 3rd highest CAS latency (not supported, see byte 18)	00
27	DDR2 SDRAM Device Minimum Row Precharge Time t_{RP}	3C
28	DDR2 SDRAM Device Minimum Row Active to Row Active t_{RRD}	1E
29	DDR2 SDRAM Device Minimum RAS# to CAS# Delay t_{RCD}	3C
30	DDR2 SDRAM Device Minimum RAS# Pulse Width t_{RAS}	2D
31	Module Rank Density (see DDR2 SPD standard for value definitions)	40
32	DDR2 SDRAM Device Command and Address signal input setup time t_{IS}	60
33	DDR2 SDRAM Device Command and Address signal input hold time t_{IH}	60
34	DDR2 SDRAM Device Data signal input setup time t_{DS}	40

Table 6: DDR2 SDRAM Serial Presence Detect Table

Hex values shown are representative

BYTE NUMBER	FUNCTION DESCRIBED	SPD HEX VALUE
35	DDR2 SDRAM Device Data signal input hold time t_{DH}	40
36	DDR2 SDRAM Device Write Recovery time t_{WR}	3C
37	DDR2 SDRAM Device Internal write to read command delay t_{WTR}	28
38	DDR2 SDRAM Device Internal read to precharge command delay t_{RTP}	1E
39	Memory Analysis Probe Characteristics	00
40	Extension for byte 41 and byte 42 (see DDR2 SPD standard for value definitions)	00
41	DDR2 SDRAM Device Minimum Active to Active/Auto Refresh Time t_{RC}	3C
42	DDR2 SDRAM Device Minimum Auto-Refresh to Active/Auto-Refresh t_{RFC}	4B
43	DDR2 SDRAM Device Maximum device cycle time t_{CKMAX}	80
44	DDR2 SDRAM Device Maximum skew between DQS and DQ signals t_{DQSQ}	23
45	DDR2 SDRAM Device Maximum Read DataHold Skew Factor t_{QHS}	2D
46	PLL Relock Time	00 or 0F
47-61	RESERVED	01
62	SPD Revision (current rev, 1.0)	10
63	Checksum for Bytes 0-62	Calculated
64	Manufacturer's JEDEC ID Code (Micron's is 44)	2C
65-71	Manufacturer's JEDEC ID Code (Continued)	FF
72	Module Manufacturing Location	01-0C
73-90	Module Part Number	Variable
91	PCB Identification Code	01-09
92	PCB Identification Code (Continued)	00
93	Year of Manufacture	Variable
94	Week of Manufacture	Variable
95-98	Module Serial Number	Variable
99-127	Manufacturer's Specific Data	Variable
128-255	Open for customer use	FF

Conclusion

Over time, the complexity of memory has increased; moving from parallel presence-detect to the more flexible serial presence-detect has proved to be a critical innovation. As DRAM technology has progressed from fastpage/EDO to DDR2, SPD data requirements have

also grown. This is shown by the increase in populated SPD bytes and the level of performance data the SPD needs to provide to the system BIOS. The next step in DRAM technology, DDR3, will continue this SPD growth pattern.



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